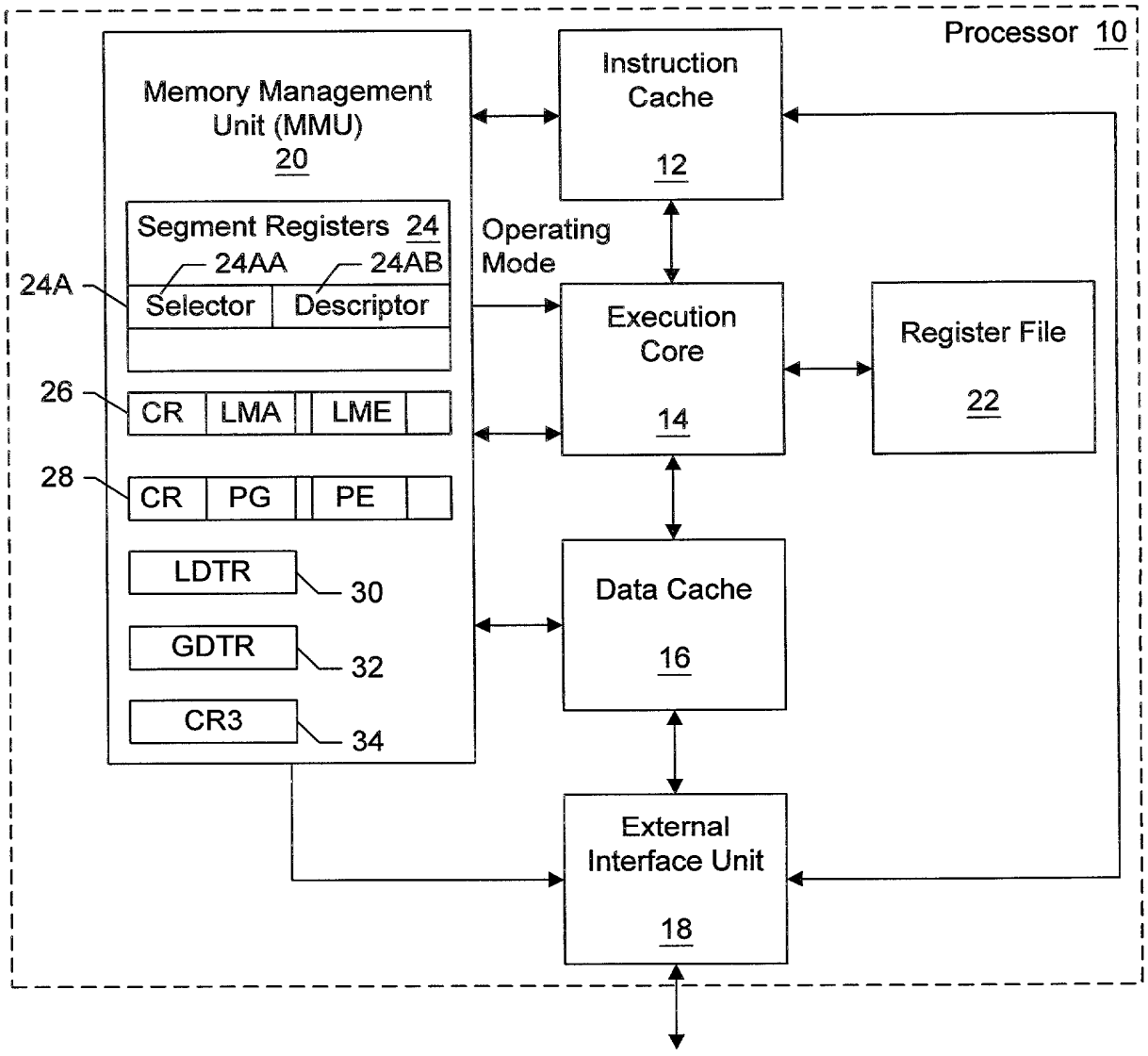
Processor 10
Memory Management Unit (MMU) 20
Segment Registers 24
24AA
24AB
24A
Selector
Descriptor
26
CR
LMA
LME
28
CR
PG
PE
LDTR
30
GDTR
32
CR3
34
Instruction Cache 12
Operating Mode
Execution Core 14
Register File 22
Data Cache 16
External Interface Unit 18

Fig. 1

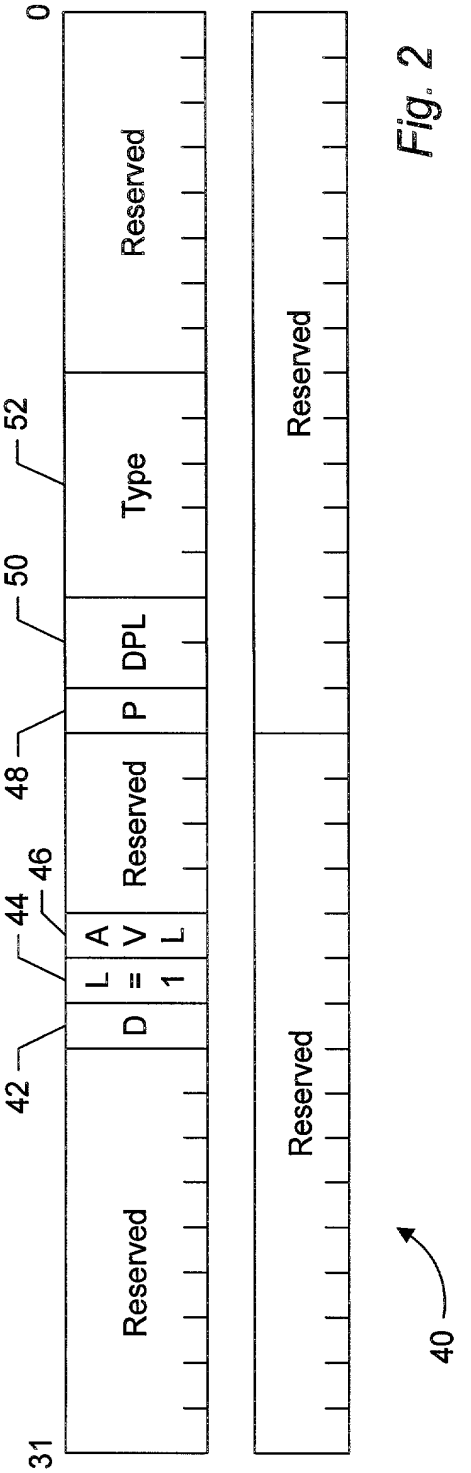
0
31
Reserved
D = 1
L
A
V
L
Reserved
P
DPL
Type
Reserved
42
44
46
48
50
52
Reserved
40

Fig. 2

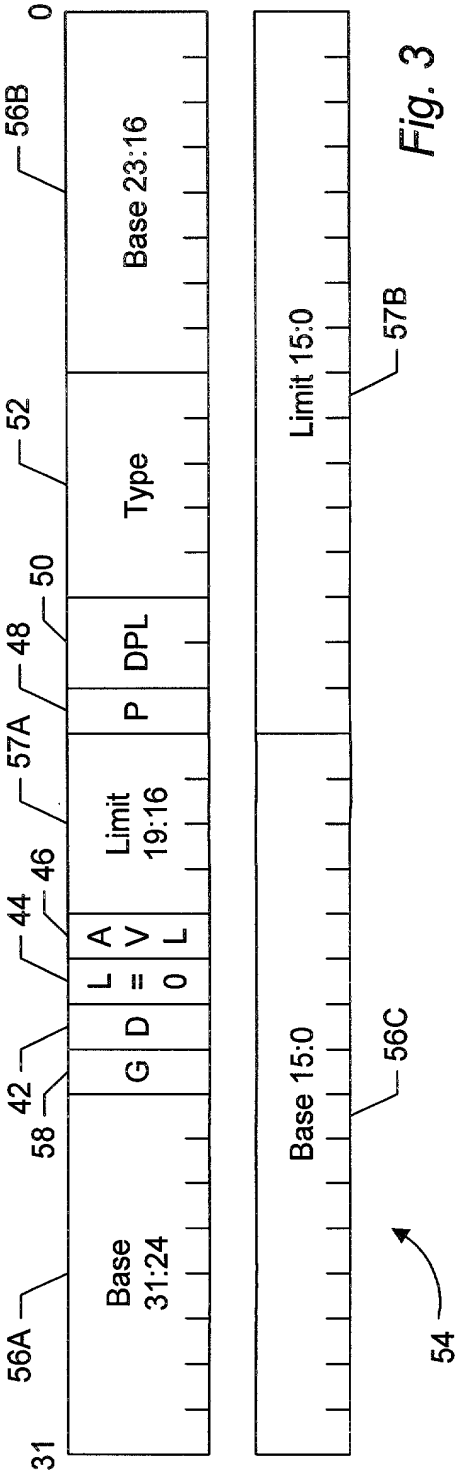
0
31
Base 31:24
G
D
= 0
L
A
V
L
Limit 19:16
P
DPL
Type
Base 23:16
Base 15:0
Limit 15:0
42
44
46
48
50
52
56A
56B
56C
57A
57B
58
54

Fig. 3

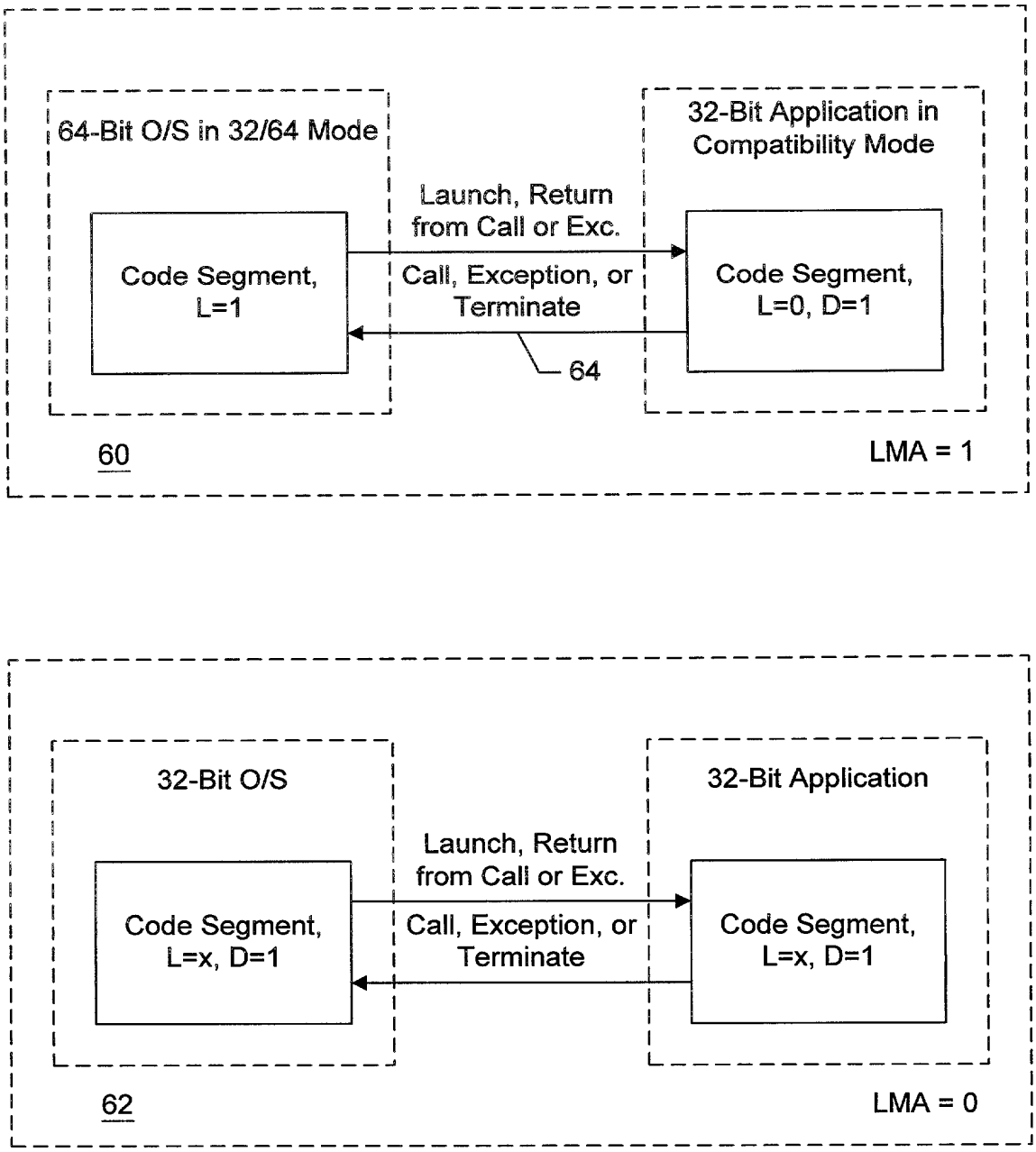
64-Bit O/S in 32/64 Mode
32-Bit Application in Compatibility Mode
Launch, Return from Call or Exc.
Code Segment, L=1
Call, Exception, or Terminate
Code Segment, L=0, D=1
64
60
LMA = 1
32-Bit O/S
32-Bit Application
Launch, Return from Call or Exc.
Code Segment, L=x, D=1
Call, Exception, or Terminate
Code Segment, L=x, D=1
62
LMA = 0

Fig. 4

LMA	CS L Bit	CS D Bit	Operating Mode
0	x	0	16 Bit Mode
0	x	1	32 Bit Mode
1	0	0	16 Bit Compatibility Mode
1	0	1	32 Bit Compatibility Mode
1	1	0	32/64 Mode
1	1	1	Reserved

70

Fig. 5

Override Prefix		None	REX	(66H , 67H)
32/64 Mode	Operand Size	32 bits	64 bits	16 bits
	Address Size	64 bits	DNA	32 bits
32 Bit Mode Incl. Compatibility Mode	Operand Size	32 bits	DNA	16 bits
	Address Size	32 bits	DNA	16 bits
16 Bit Mode Incl. Compatibility Mode	Operand Size	16 bits	DNA	32 bits
	Address Size	16 bits	DNA	32 bits

72

Fig. 6

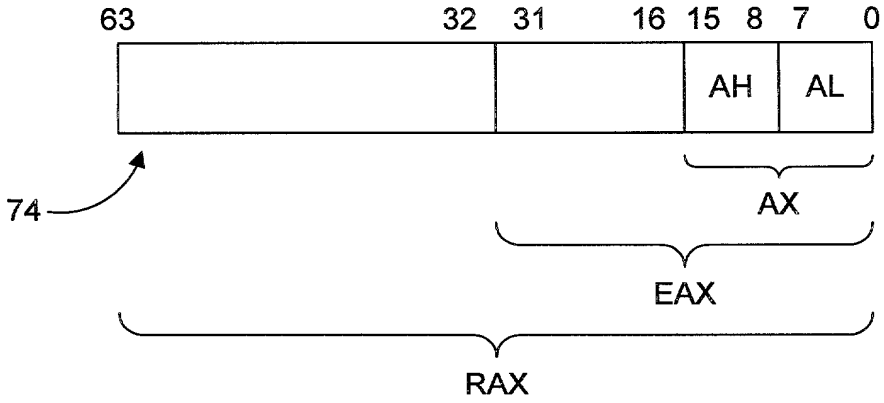

Fig. 7

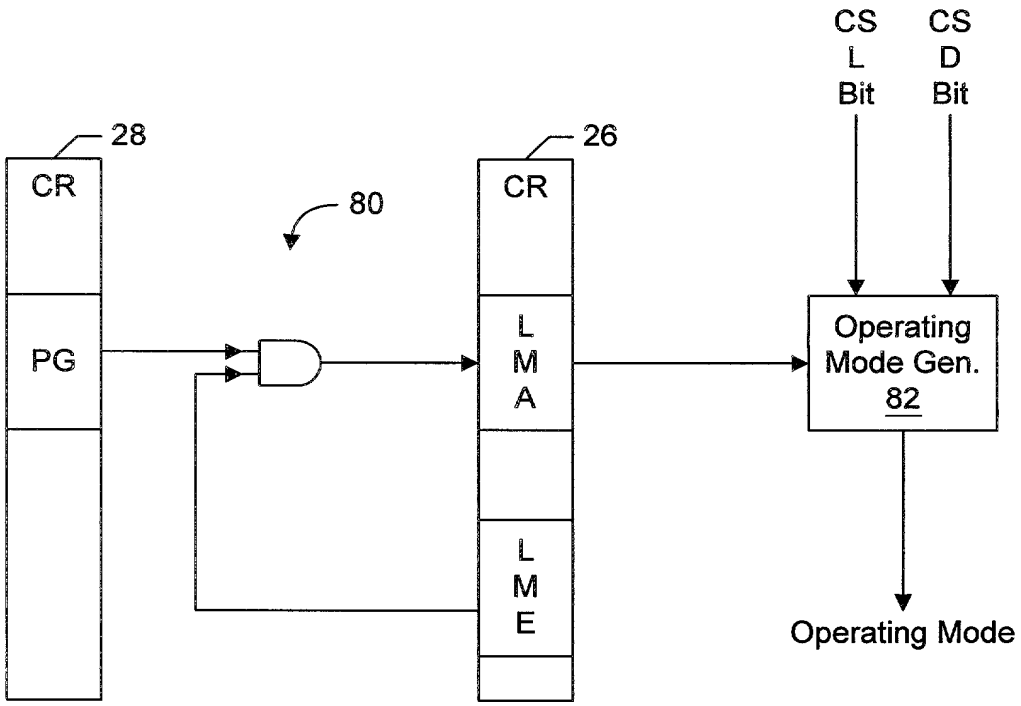
CS
L
Bit
CS
D
Bit
28
CR
PG
80
26
CR
L
M
A
L
M
E
Operating
Mode Gen.
82
Operating Mode

Fig. 8

Change	Check
LME 0 → 1	If PG=1 then exception
LME 1 → 0	If PG=1 then exception
PG 0 → 1	If LME=1 and PAE=0 then exception
PAE 1 → 0	If LMA=1 then exception

90

Fig. 9

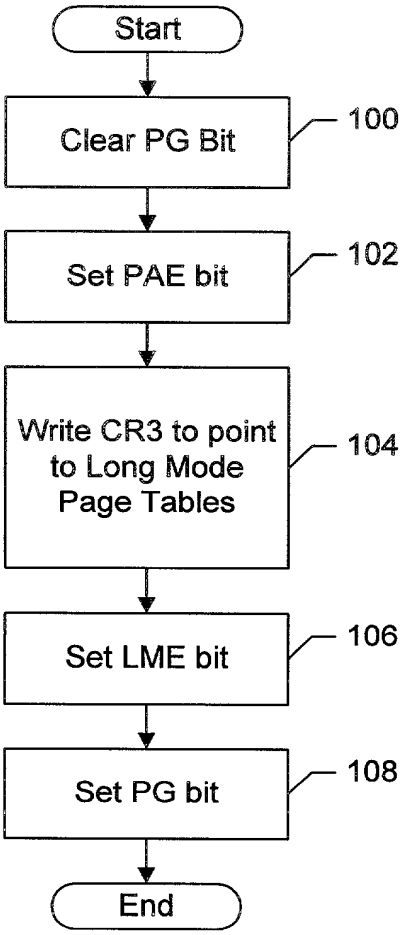
Start
Clear PG Bit
100
Set PAE bit
102
Write CR3 to point to Long Mode Page Tables
104
Set LME bit
106
Set PG bit
108
End

Fig. 10

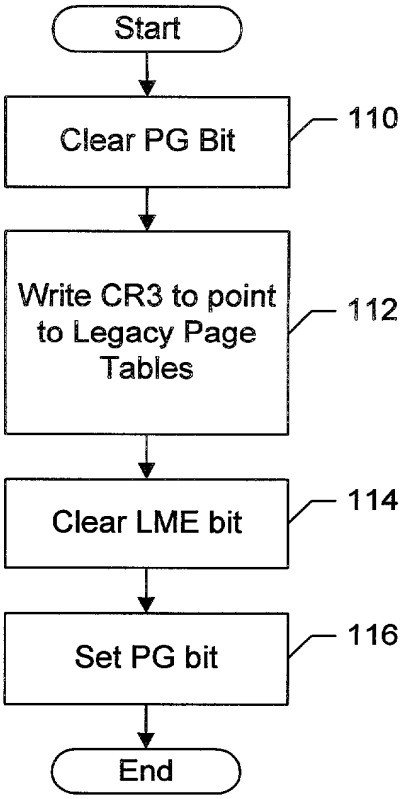
Start
Clear PG Bit
110
Write CR3 to point to Legacy Page Tables
112
Clear LME bit
114
Set PG bit
116
End

Fig. 11

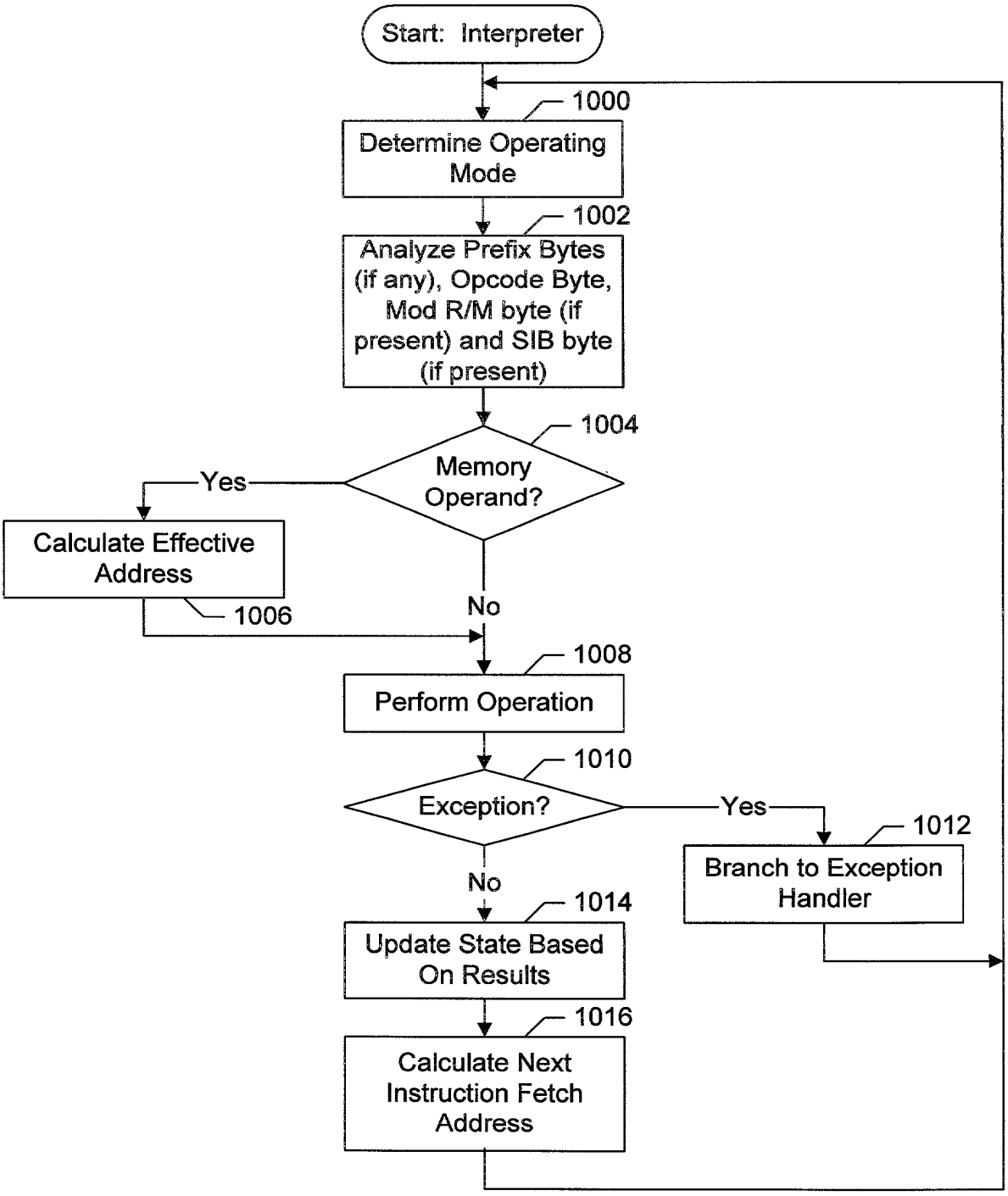
Start: Interpreter
1000
Determine Operating Mode
1002
Analyze Prefix Bytes (if any), Opcode Byte, Mod R/M byte (if present) and SIB byte (if present)
1004
Memory Operand?
Yes
Calculate Effective Address
1006
No
1008
Perform Operation
1010
Exception?
Yes
1012
Branch to Exception Handler
No
1014
Update State Based On Results
1016
Calculate Next Instruction Fetch Address

Fig. 12

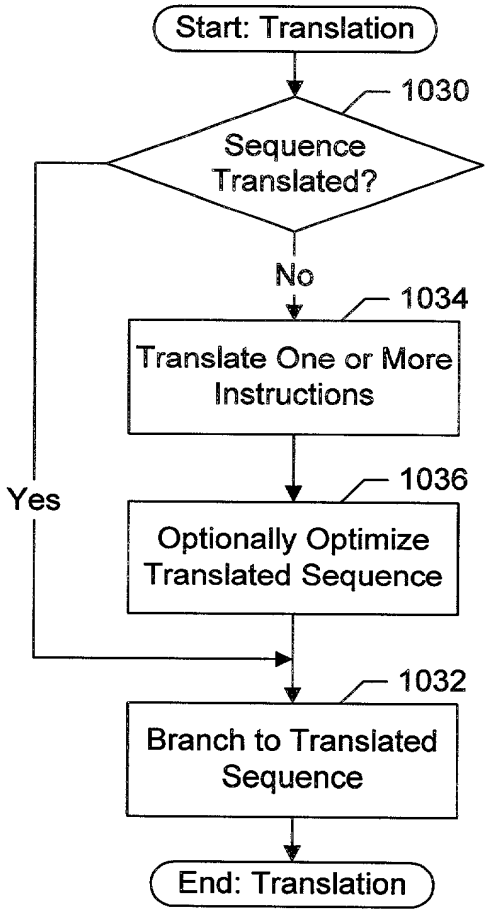
Start: Translation
1030
Sequence Translated?
No
1034
Translate One or More Instructions
1036
Optionally Optimize Translated Sequence
Yes
1032
Branch to Translated Sequence
End: Translation

Fig. 13

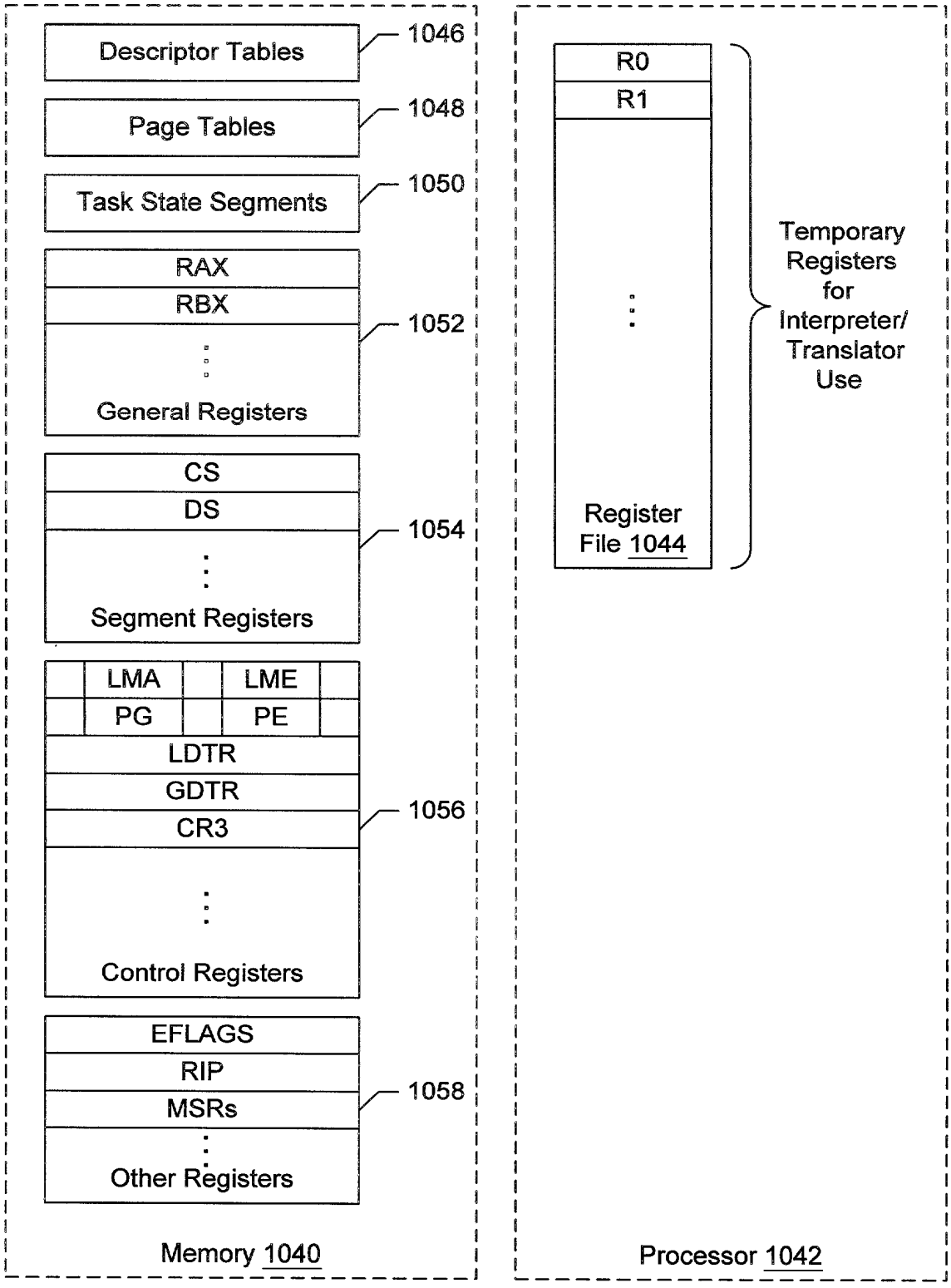
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
RAX
RBX
General Registers
1052
CS
DS
Segment Registers
1054
LMA
LME
PG
PE
LDTR
GDTR
CR3
Control Registers
1056
EFLAGS
RIP
MSRs
Other Registers
1058
Memory 1040
R0
R1
Register File 1044
Temporary Registers for Interpreter/ Translator Use
Processor 1042

Fig. 14

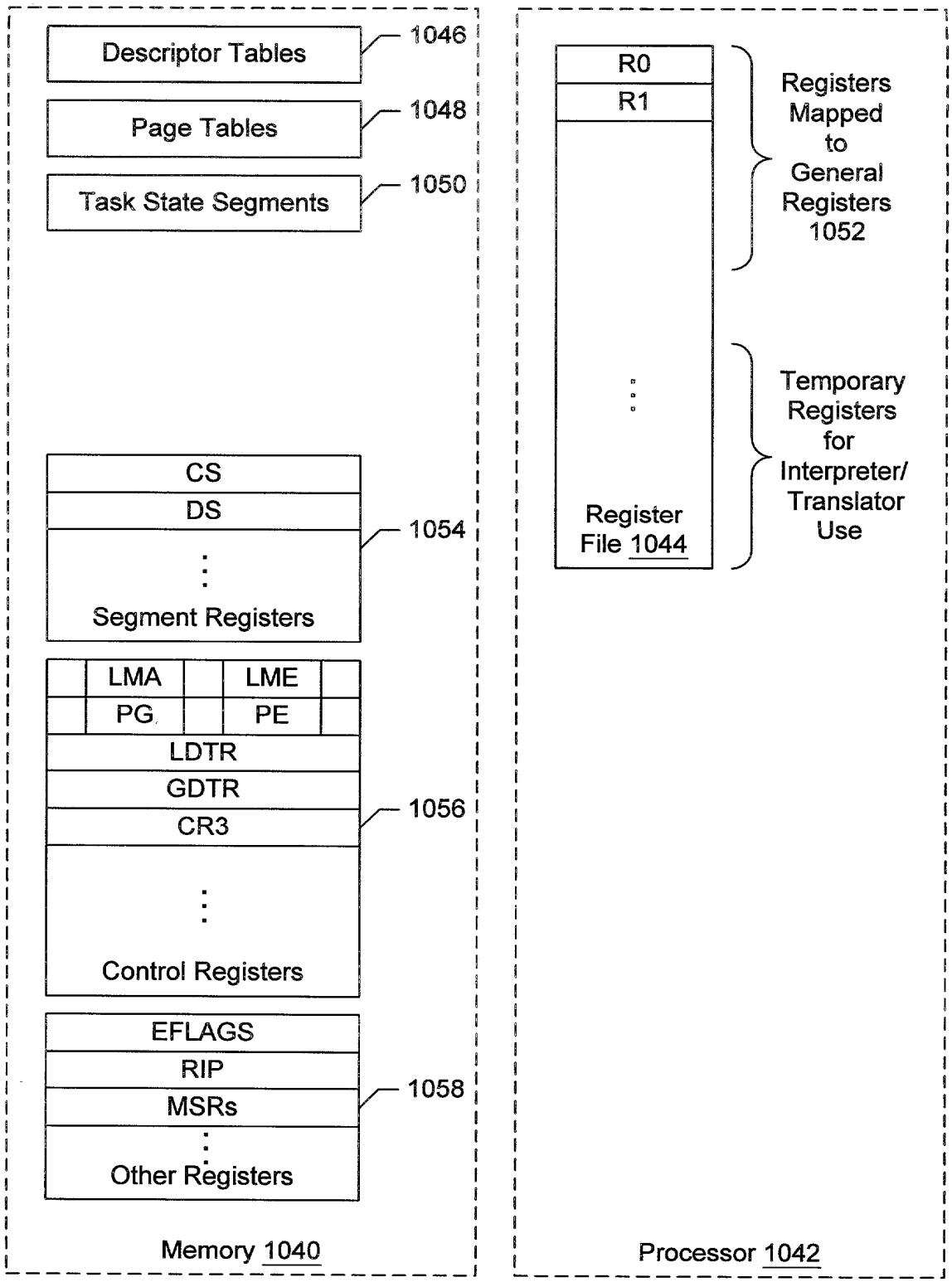
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
CS
DS
Segment Registers
1054
LMA
LME
PG
PE
LDTR
GDTR
CR3
1056
Control Registers
EFLAGS
RIP
MSRs
Other Registers
1058
Memory 1040
R0
R1
Register File 1044
Registers Mapped to General Registers 1052
Temporary Registers for Interpreter/ Translator Use
Processor 1042

Fig. 15

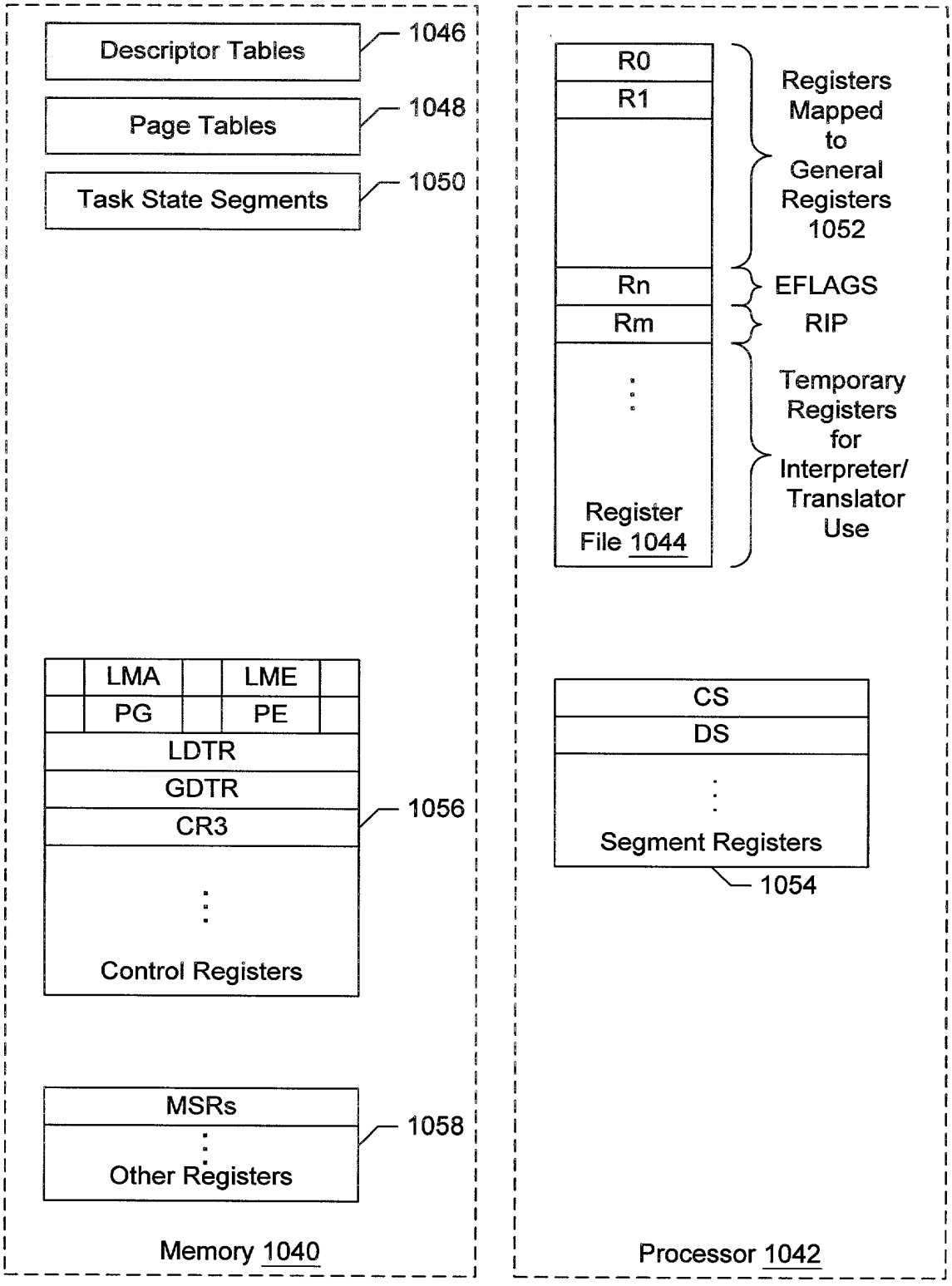
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
LMA
LME
PG
PE
LDTR
GDTR
CR3
1056
Control Registers
MSRs
1058
Other Registers
Memory 1040
R0
R1
Registers Mapped to General Registers 1052
Rn
EFLAGS
Rm
RIP
Temporary Registers for Interpreter/ Translator Use
Register File 1044
CS
DS
Segment Registers
1054
Processor 1042

Fig. 16

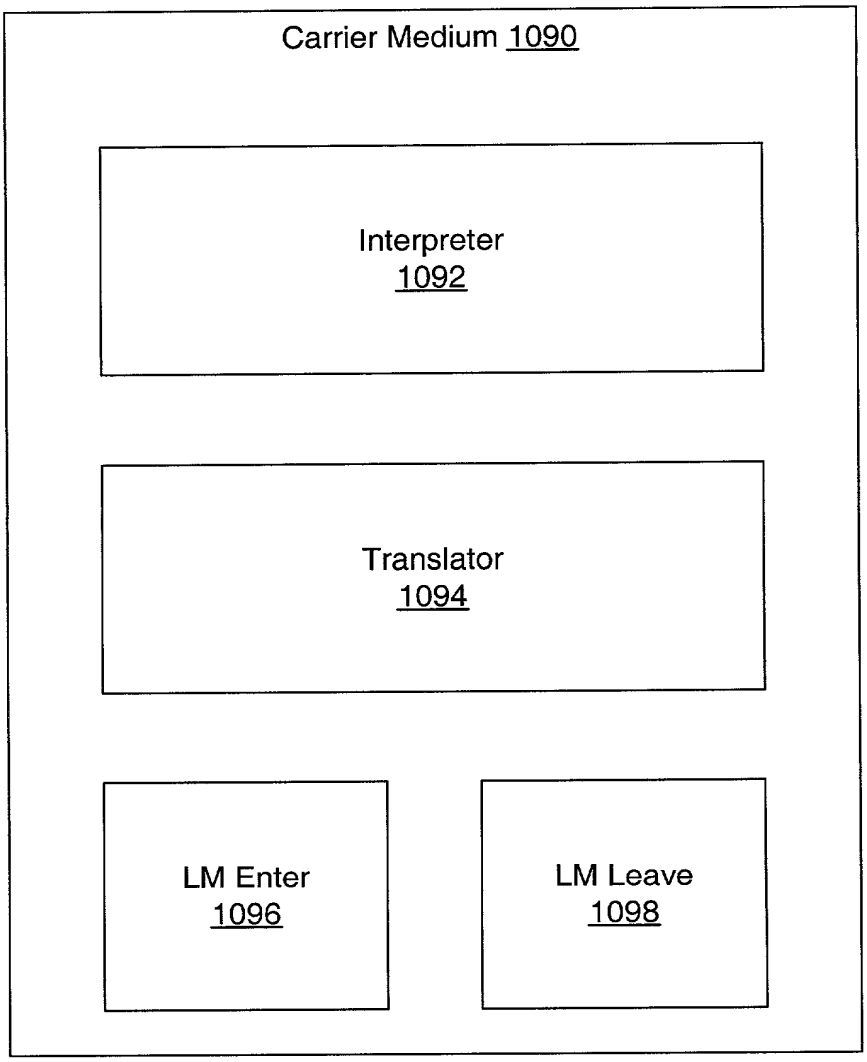
Carrier Medium 1090
Interpreter
1092
Translator
1094
LM Enter
1096
LM Leave
1098

Fig. 17

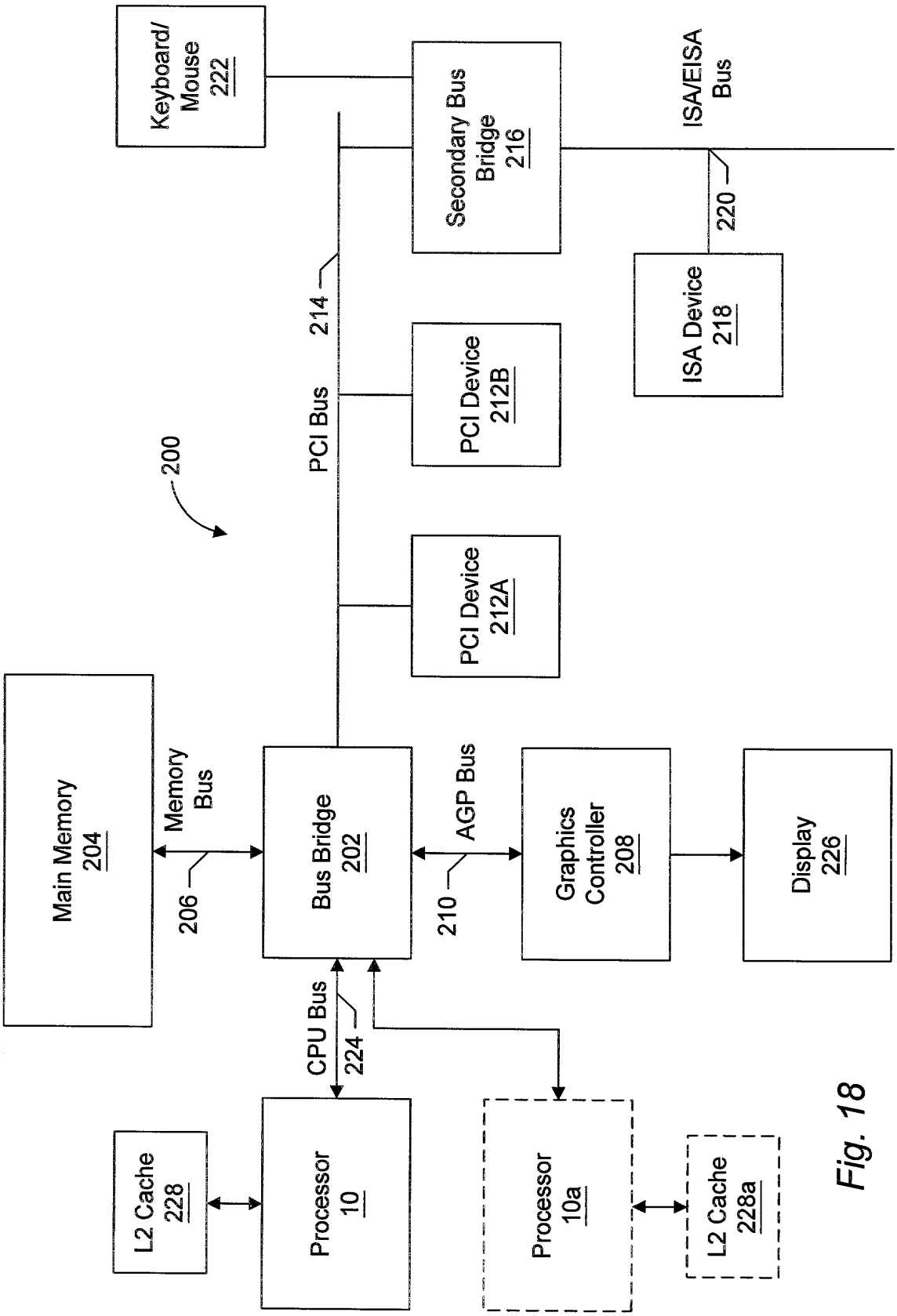
Keyboard/ Mouse 222
Secondary Bus Bridge 216
ISA/EISA Bus
220
ISA Device 218
214
PCI Bus
PCI Device 212B
PCI Device 212A
200
Main Memory 204
Memory Bus
206
Bus Bridge 202
AGP Bus
210
Graphics Controller 208
Display 226
CPU Bus
224
L2 Cache 228
Processor 10
Processor 10a
L2 Cache 228a

Fig. 18

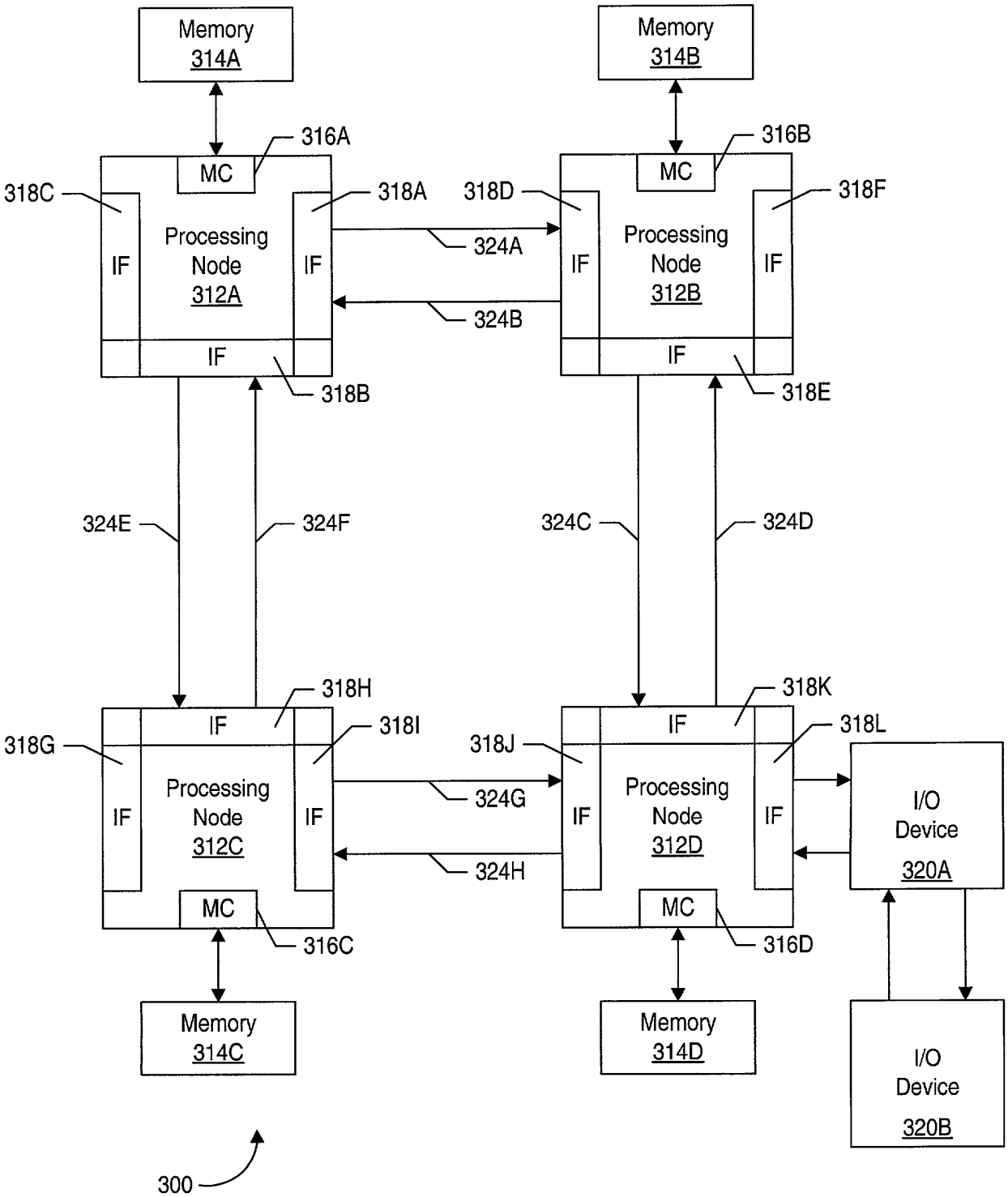
Memory
314A
Memory
314B
316A
316B
MC
MC
318C
318A
318D
318F
IF
Processing
Node
312A
IF
IF
Processing
Node
312B
IF
324A
324B
IF
IF
318B
318E
324E
324F
324C
324D
318H
318K
IF
IF
318G
318I
318J
318L
IF
Processing
Node
312C
IF
IF
Processing
Node
312D
IF
324G
324H
I/O
Device
320A
MC
MC
316C
316D
Memory
314C
Memory
314D
I/O
Device
320B
300

Fig. 19